



INFORMATION DISCLOSURE CITATION

Atty. Docket No. 06720.0074	Appln. No. 09/987,616
Applicant Ming-Duo KER et al.	
Filing Date November 15, 2001	Group: 2836

U.S. PATENT DOCUMENTS						
Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
b6	5,453,384	09/26/1995	Chatterjee	437	6	
	5,502,328	03/26/1996	Chen et al.	257	546	
	5,581,104	12/03/1996	Lowrey et al.	257	355	
	5,629,544	05/13/1997	Voldman et al.	257	355	
	5,654,862	08/05/1997	Worley et al.	361	111	
	5,719,737	02/17/1998	Maloney	361	111	
	5,807,791	09/15/1998	Bertin et al.	438	738	
	5,907,462	05/25/1999	Chatterjee et al.	361	56	
	5,932,918	08/03/1999	Krakauer	257	368	
	5,940,258	08/17/1999	Duvvury	361	56	
	5,990,520	11/23/1999	Noorlag et al.	257	362	
	6,015,992	01/18/2000	Chatterjee et al.	257	350	
	6,034,397	03/07/2000	Voldman	257	335	

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FOREIGN PATENT DOCUMENTS							
		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
b6	S. Voldman et al., "Semiconductor Process and Structural Optimization of Shallow Trench Isolation-Defined and Polysilicon-Bound Source/Drain Diodes for ESD Networks", EOS/ESD SYMPOSIUM PROCEEDINGS, 1998, pp. 98-151 through 98-160.
b6	Steven H. Voldman et al., "Analysis of Snubber-Clamped Diode-String Mixed Voltage Interface ESD Protection Network for Advanced Microprocessors", EOS/ESD SYMPOSIUM PROCEEDINGS 1995, pp. 95-43 through 95-61.
b6	Marcel J. M. Pelgrom et al., "A 3/5 V Compatible I/O Buffer", IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 30, No. 7, July 1995, pp. 823-825.



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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)			
		Héctor Sánchez et al., "A Versatile 3.3/2.5/1.8-V CMOS I/O Driver Built in a 0.2- μ m, 3.5-nm Tox, 1.8-V CMOS Technology", IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 34, No. 11, November 1999, pp. 1501-1511.	
		Gajendra P. Singh et al., "High-Voltage-Tolerant I/O Buffers With Low-Voltage CMOS Process", IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 34, No. 11, November 1999, pp. 1512-1525.	
		C. Richier et al., "Investigation on Different ESD Protection Strategies Devoted to 3.3 V RF Applications (2 Ghz) in a 0.18 μ m CMOS Process", EOS/ESD SYMPOSIUM PROCEEDINGS 2000, pp. 00-251 through 00-259.	
		Nishath K. Verghese et al., "Verification of RF and Mixed-Signal Integrated Circuits for Substrate Coupling Effects", IEEE 1997 CUSTOM INTEGRATED CIRCUITS CONFERENCE, 1997, pp. 363-370.	
		Ranjit Gharpurey, "A Methodology for Measurement and Characterization of Substrate Noise in High Frequency Circuits", IEEE 1998 CUSTOM INTEGRATED CIRCUITS CONFERENCE, 1998, pp. 487-490.	
		Min Xu et al., "Measuring and Modeling the Effects of Substrate Noise on the LNA for a CMOS GPS Receiver, IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 36, No. 3, March 2001, pp. 473-485.	
		Ming-Dou Ker et al., "ESD Protection Design on Analog Pin With Very Low Input Capacitance for High-Frequency or Current-Mode Applications", IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 35, No. 8, August 2000, pp. 1194-1199.	
		Makoto Nagata et al., "Physical Design Guides for Substrate Noise Reduction in CMOS Digital Circuits", IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 36, No. 3, March 2001, pp. 539-549.	
		Ming-Dou Ker et al., "ESD Protection Design on Analog Pin With Very Low Input Capacitance for RF or Current-Mode Applications", TWELFTH ANNUAL IEEE INTERNATIONAL ASIC/SOC CONFERENCE, 1999, pp. 352-356.	
		Ming-Dou Ker, "Whole-Chip ESD Protection Design With Efficient VDD-to-VSS ESD Clamp Circuits for Submicron CMOS VLSI", IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 46, No. 1, January 1999, pp. 173-183.	
		Tung-Yang CHEN et al., "Design on ESD Protection Circuit with Very Low and Constant Input Capacitance", PROCEEDINGS OF THE IEEE ISQED 2001, pp. 247-248.	
		Ming-Dou Ker et al., "A Gate-Coupled PTLSCR/NTLSCR ESD Protection Circuit for Deep-Submicron Low-Voltage CMOS IC's", IEEE JOURNAL OF SOLID-STATE CIRCUITS, 1997, Vol. 32, pp. 38-51.	
		Ming-Dou Ker et al., "On-Chip ESD Protection Using Capacitor-Couple Technique in 0.5- μ m CMOS Technology", Proc. 8th Int'l. ASIC Conf., Exhibit, 1995, pp. 135-138.	
		W.R. Anderson, et al., "ESD Protection for Mixed-Voltage I/O Using NMOS Transistors Stacked in a Cascode Configuration", ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE SYMPOSIUM PROCEEDINGS, 1998, pp. 98-54 through 98-62.	

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
<i>BA</i>	Ming-Duo Ker et al, "CMOS On-Chip ESD Protection Design With Substrate-Triggering Technique", IEEE INTERNATIONAL CONFERENCE ON ELECTRONICS, CIRCUITS AND SYSTEMS, 1998, Vol. 1, pp. 273-276.

Examiner	<i>Boris Benenson</i>	Date Considered	<i>7.31.03</i>
*Examiner:	Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		
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